WHAT IS CLAIMED IS:

1. A voltage controlled current source circuit comprising:

a first transistor having a control terminal coupled to a control voltage, a first terminal, and a second terminal;

a first resistor;

a first current mirror having a current terminal coupled to a first terminal of the first resistor, wherein the first current mirror generates a first reference current;

a first voltage controlled impedance circuit having a current input and a first voltage control input;

a second current mirror having a current terminal coupled to the current input of the voltage controlled impedance, wherein the second current mirror generates a second reference current; and

a second voltage controlled impedance circuit having a current input coupled to the second terminal of the first transistor, and a second voltage control input;

wherein the first reference current and the second reference current are coupled together at a voltage control node, and wherein the first and second voltage control inputs are coupled to the voltage control node.

2. The voltage controlled current source circuit of claim 1 wherein the first transistor is an NMOS transistor, the first terminal is a drain terminal, and the second terminal is a source terminal.

3. The voltage controlled current source circuit of claim 1 wherein the first resistor is an external resistor.

4. The voltage controlled current source circuit of claim 3 wherein the external resistor is a high tolerance resistor.

5. The voltage controlled current source circuit of claim 1 further comprising a third current mirror having a first current terminal coupled to receive the second reference current and a second current terminal coupled to the voltage control node.

6. The voltage controlled current source circuit of claim 1 wherein the first voltage controlled impedance comprises:

a second transistor having a control terminal coupled to the voltage control node, a first terminal coupled to the current terminal of the second current mirror, and a second terminal; and

a third transistor having a control terminal, a first terminal, and a second terminal, wherein the control terminal and first terminal of the third transistor are coupled to the current terminal of the second current mirror, and the second terminal of the third transistor is coupled to the second terminal of the second transistor.

7. The voltage controlled current source circuit of claim 1 wherein the second voltage controlled impedance comprises:

a second transistor having a control terminal coupled to the voltage control node, a first terminal coupled to the second terminal of the first transistor, and a second terminal; and

a third transistor having a control terminal, a first terminal, and a second terminal, wherein the control terminal and first terminal of the third transistor are coupled to the second terminal of the first transistor, and the second terminal of the third transistor is coupled to the second terminal of the second transistor.

8. The voltage controlled current source circuit of claim 1 wherein first current mirror has a current ratio of M:N.

9. A voltage controlled current source circuit comprising:

a first resistor;

a first current mirror having a current terminal coupled to a first terminal of the first resistor, wherein the first current mirror generates a first reference current;

a first voltage controlled impedance circuit having a current input and a first voltage control input; and

a second current mirror having a current terminal coupled to the current input of the voltage controlled impedance, wherein the second current mirror generates a second reference current;

wherein the first reference current and the second reference current are coupled together at a voltage control node, and wherein the first voltage control input is coupled to the voltage control node.

10. The voltage controlled current source circuit of claim 9 wherein the first reference current is directed into the voltage controlled node and the second reference current is directed out of the voltage controlled node.

11. The voltage controlled current source circuit of claim 9 wherein the first reference current is directed out of the voltage controlled node and the second reference current is directed into of the voltage controlled node.

12. The voltage controlled current source circuit of claim 9 wherein the first resistor is an external resistor.

13. The voltage controlled current source circuit of claim 9 further comprising a third current mirror having a first current terminal coupled to receive the second reference current and a second current terminal coupled to the voltage control node.

14. The voltage controlled current source circuit of claim 9 wherein the first voltage controlled impedance comprises:

a second transistor having a control terminal coupled to the voltage control node, a first terminal coupled to the current terminal of the second current mirror, and a second terminal; and

a third transistor having a control terminal, a first terminal, and a second terminal, wherein the control terminal and first terminal of the third transistor are coupled to the current terminal of the second current mirror, and the second terminal of the third transistor is coupled to the second terminal of the second transistor.

15. A voltage controlled current source circuit comprising:

a first precision reference current coupled to a voltage control node;

a first voltage controlled impedance circuit having a current input and a first voltage control input; and

a first current mirror having a first current terminal coupled to the current input of the first voltage controlled impedance, and a second current terminal, wherein the first current mirror generates a second reference current on the second current terminal;

wherein the first precision reference current and the second reference current are coupled together at the voltage control node, and wherein the first voltage control input is coupled to the voltage control node.

16. The voltage controlled current source circuit of claim 15 further comprising a second current mirror and a resistor to generate the first precision reference current.

17. The voltage controlled current source circuit of claim 15 further comprising a third current mirror to couple the second reference current to the voltage control node.

18. A voltage controlled current source circuit comprising:

a first PMOS transistor coupled between a supply voltage and a first node, the first PMOS transistor including a control terminal coupled to the first node;

a first resistor coupled between the first node and a reference voltage;

a second PMOS transistor coupled between the supply voltage and a voltage control node, the second PMOS transistor including a control terminal coupled to the control terminal of the first PMOS transistor;

a first NMOS transistor having a control terminal coupled to the voltage control node, a drain coupled to a second node, and a source;

a second NMOS transistor having a control terminal, a drain, and a source, wherein the control terminal and drain are coupled to the second node, and the source of the first NMOS transistor is coupled to the source of the second NMOS transistor;

a third PMOS transistor coupled between the supply voltage and the second node, the third PMOS transistor including a control terminal coupled to the second node;

a fourth PMOS transistor having a control terminal coupled to the control terminal of the first PMOS transistor, a source coupled to the supply voltage, and a drain; and

a current mirror having a first current terminal coupled to the drain of the fourth PMOS transistor and a second current terminal coupled to the voltage control node.

19. The voltage controlled current source circuit of claim 18 wherein the first resistor is an external high tolerance resistor.

20. The voltage controlled current source circuit of claim 18 wherein the reference voltage is ground.

21. The voltage controlled current source circuit of claim 18 wherein the source of the first NMOS transistor and the source of the second NMOS transistor are coupled to the reference voltage.

22. The voltage controlled current source circuit of claim 18 further comprising:

a third NMOS transistor having a control terminal coupled to a control voltage, a drain, and a source;

a fourth NMOS transistor having a control terminal coupled to the voltage control node, a drain coupled to the source of the third NMOS transistor, and a source; and

a fifth NMOS transistor having a control terminal, a drain, and a source, wherein the control terminal and drain are coupled to the source of the third transistor, and the source of the fourth NMOS transistor is coupled to the source of the fifth NMOS transistor.

23. A method of controlling a current comprising:

generating a first current through a resistor;

generating a second current at a current input of a voltage controlled impedance;

providing reproductions of the first current and the second current at a voltage control node to generate a first control voltage at the voltage control node; and

coupling the first control voltage at the voltage control node to a voltage input of the voltage controlled impedance, wherein the first control voltage corresponds to the difference between the first current and the second current.

24. The method of claim 23 wherein providing reproductions of the first current and the second current comprises:

reproducing the first current in a first current mirror to produce a first reference current; and

reproducing the second current in a second current mirror to produce a second reference current.

25. The method of claim 24 wherein the first reference current and the second reference current are of opposite polarity.

26. The method of claim 23 further comprising:

receiving a control voltage at the control terminal of a transistor, the transistor having a first terminal and a second terminal; and

coupling the first control voltage at the voltage control node to a voltage input of a second voltage controlled impedance, wherein a current input of the second voltage controlled impedance is coupled to the second terminal of the transistor.